

Figure 1
Different hint extension instructions.

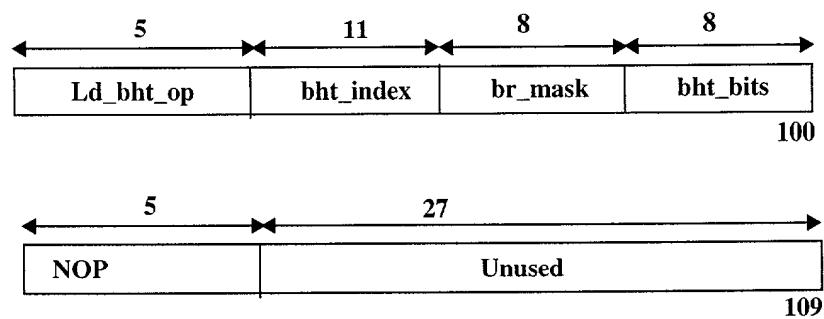


Figure 2

Overview of the Processor operation with Hint processor

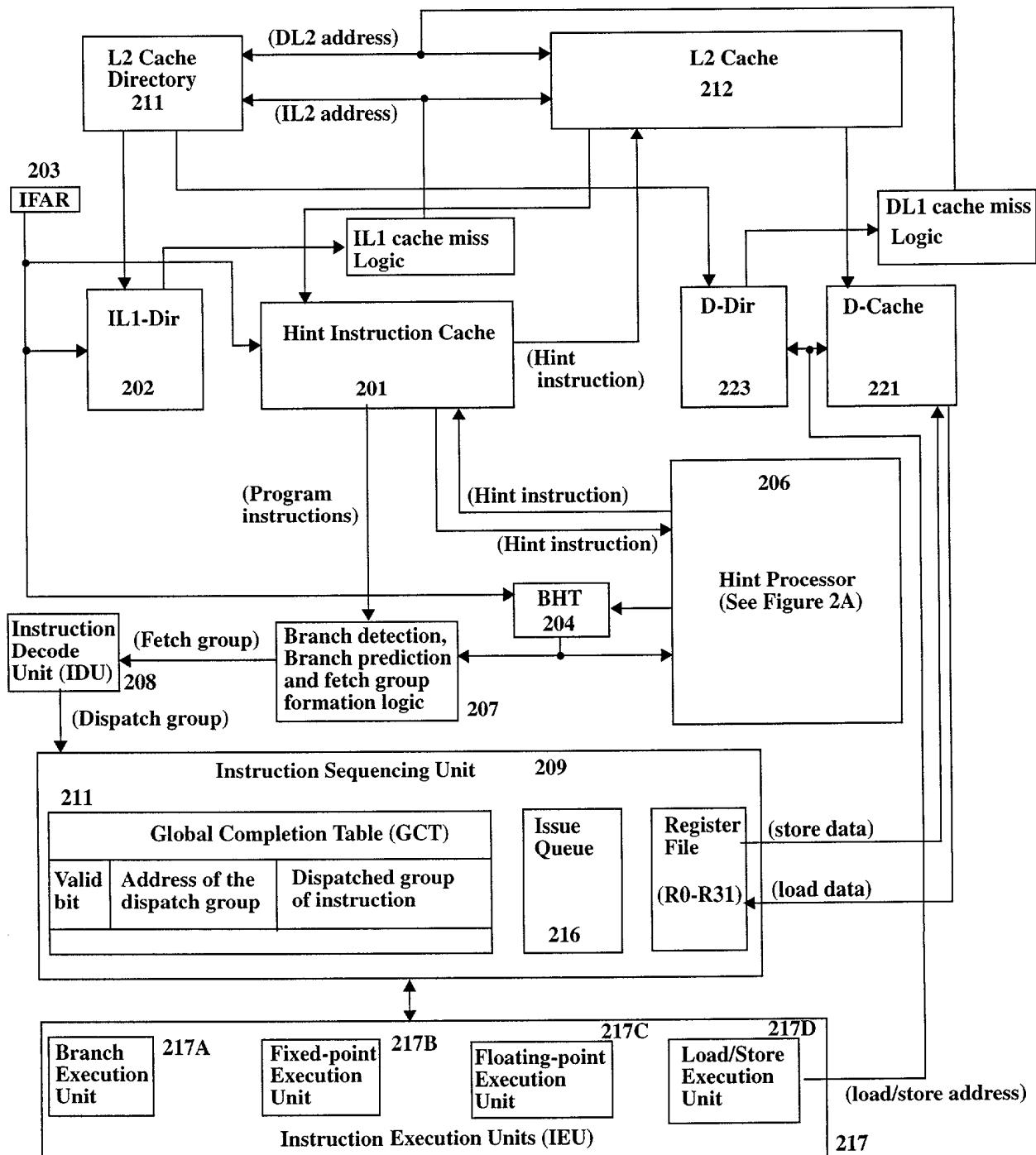


Figure 2A The Hint Processor

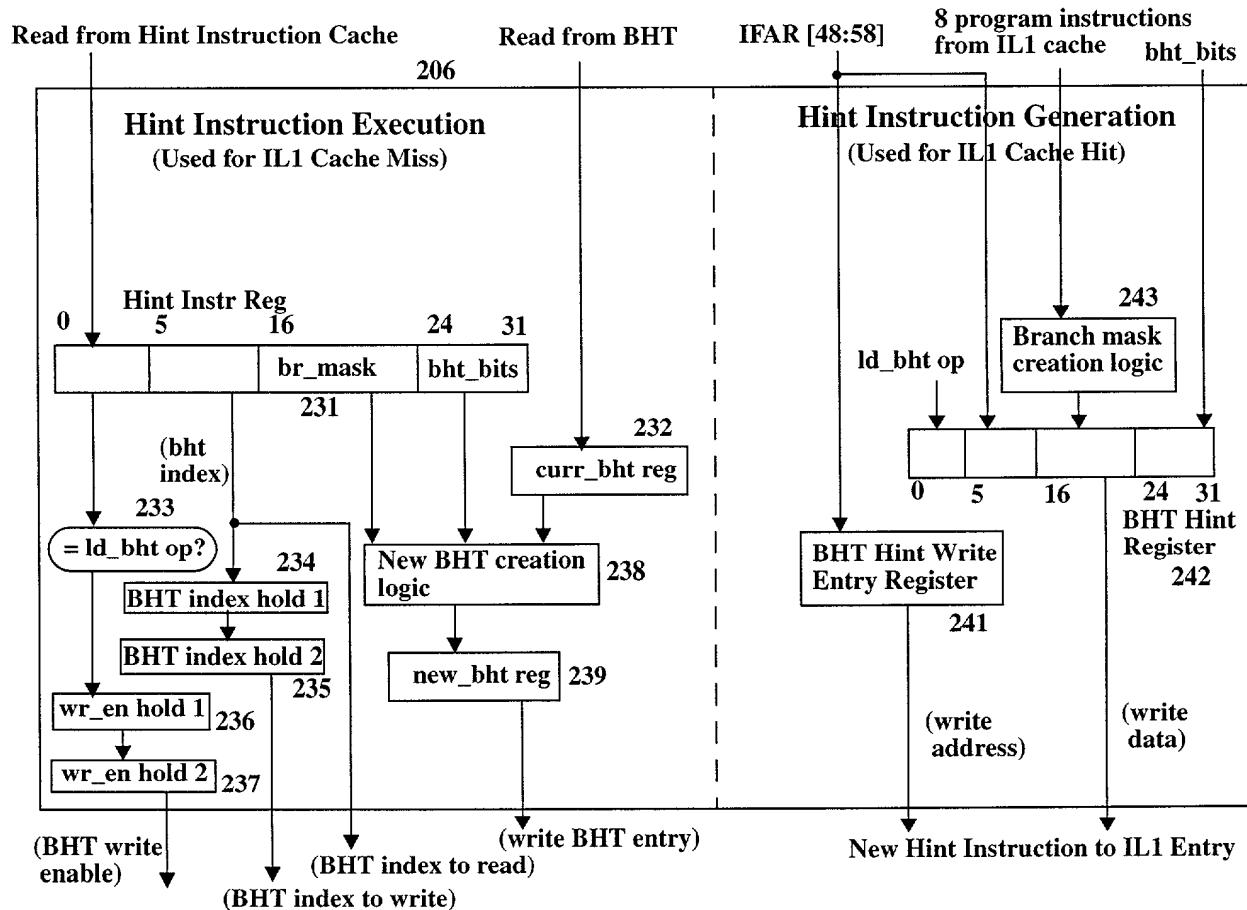


Figure 2B New BHT creation logic 238

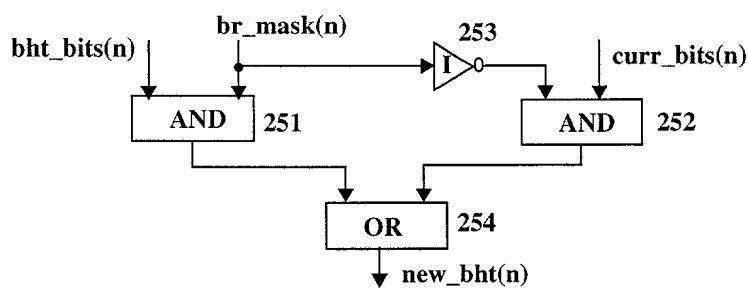


Figure 3

Overview of the Instruction Fetch Unit with Hint Processor

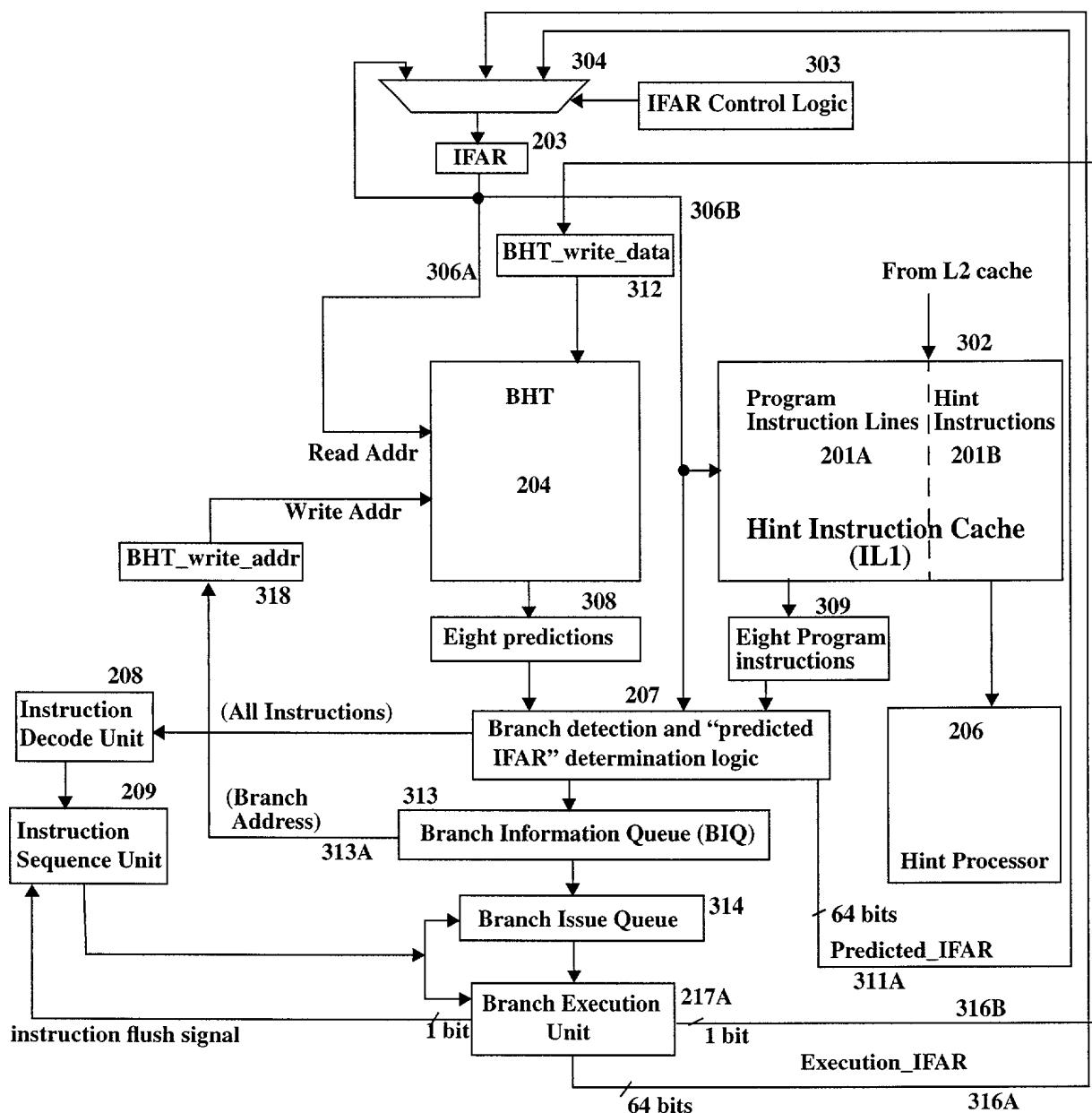


Figure 4

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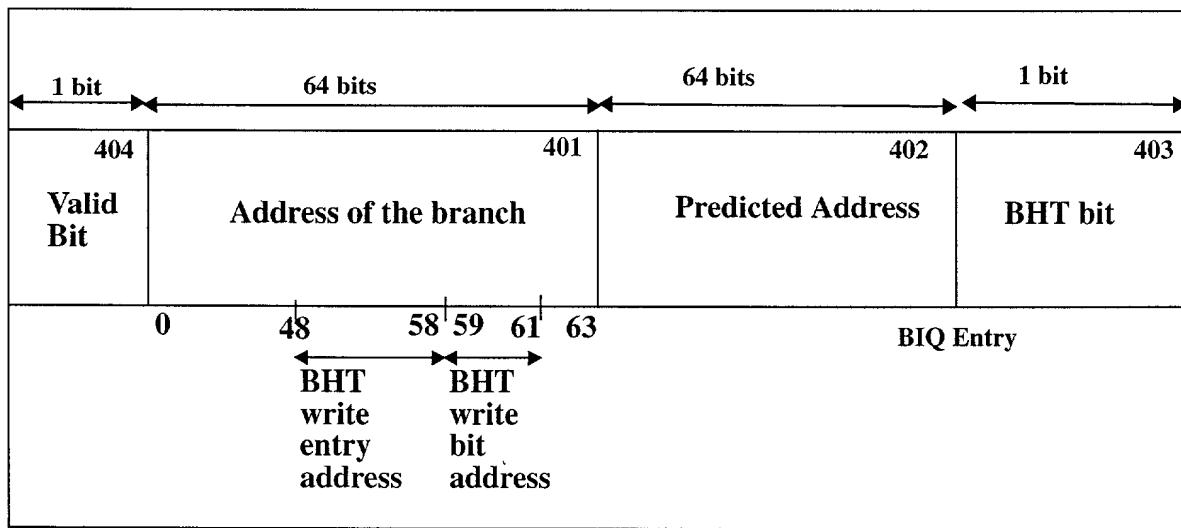
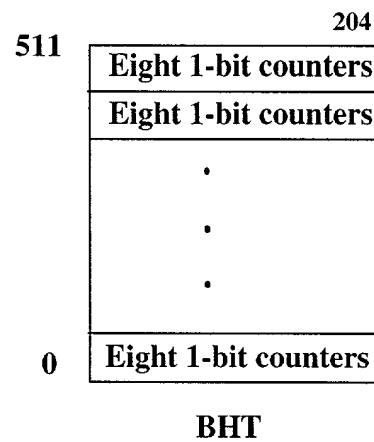
**Branch Information Queue (BIQ)****Figure 5****BHT**

Figure 6

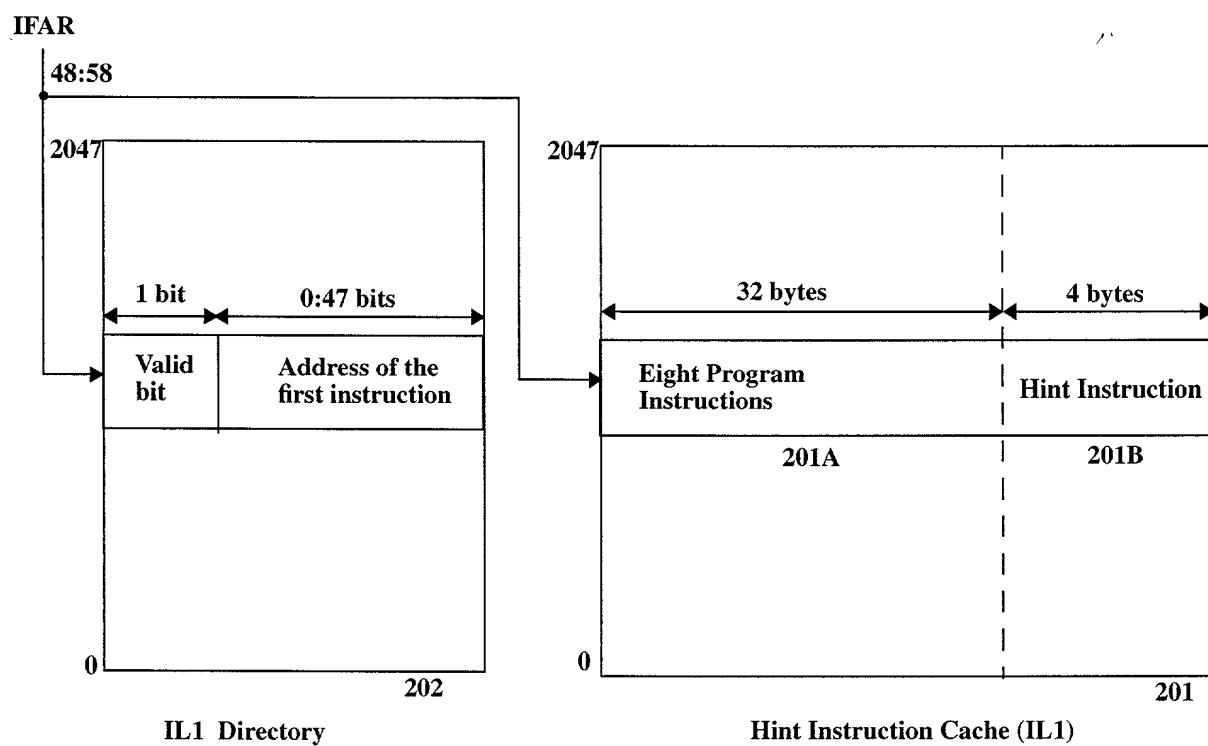


Figure 7

IL2 address

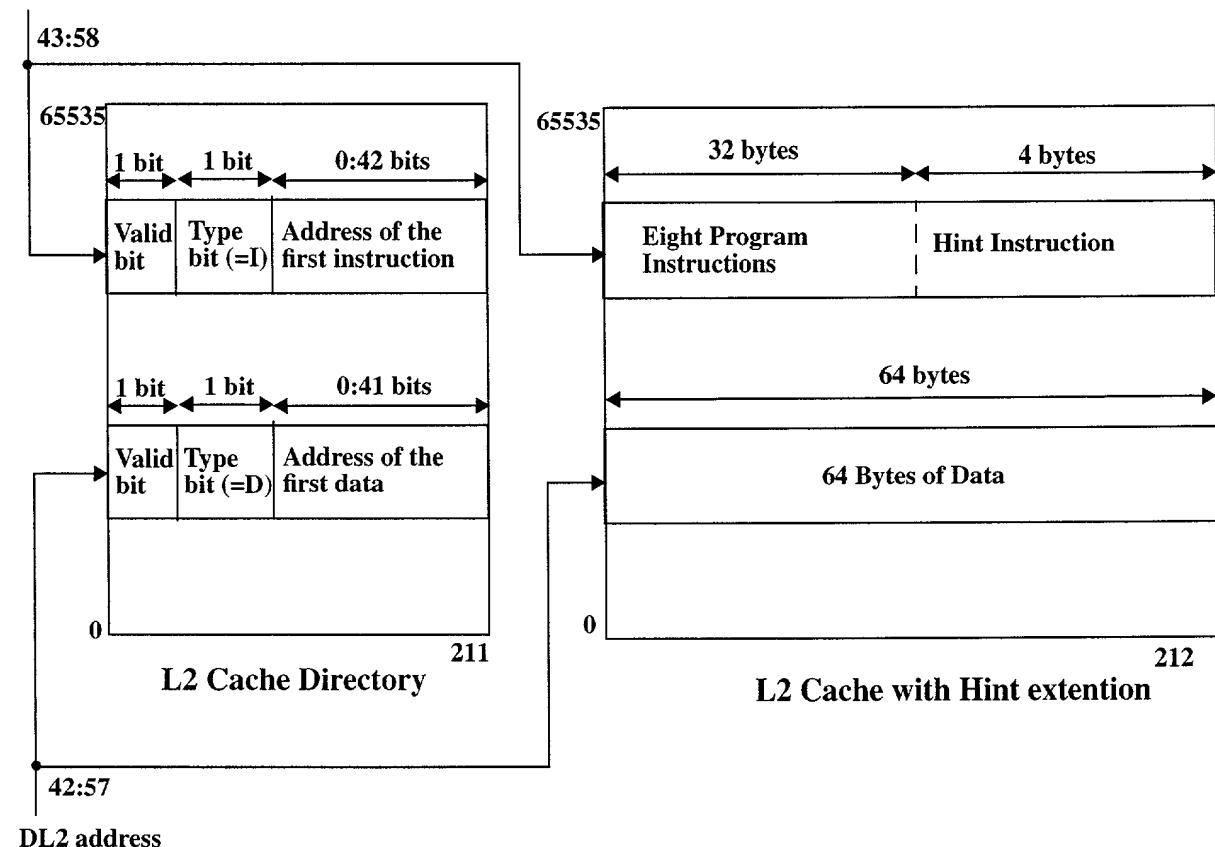


Figure 8

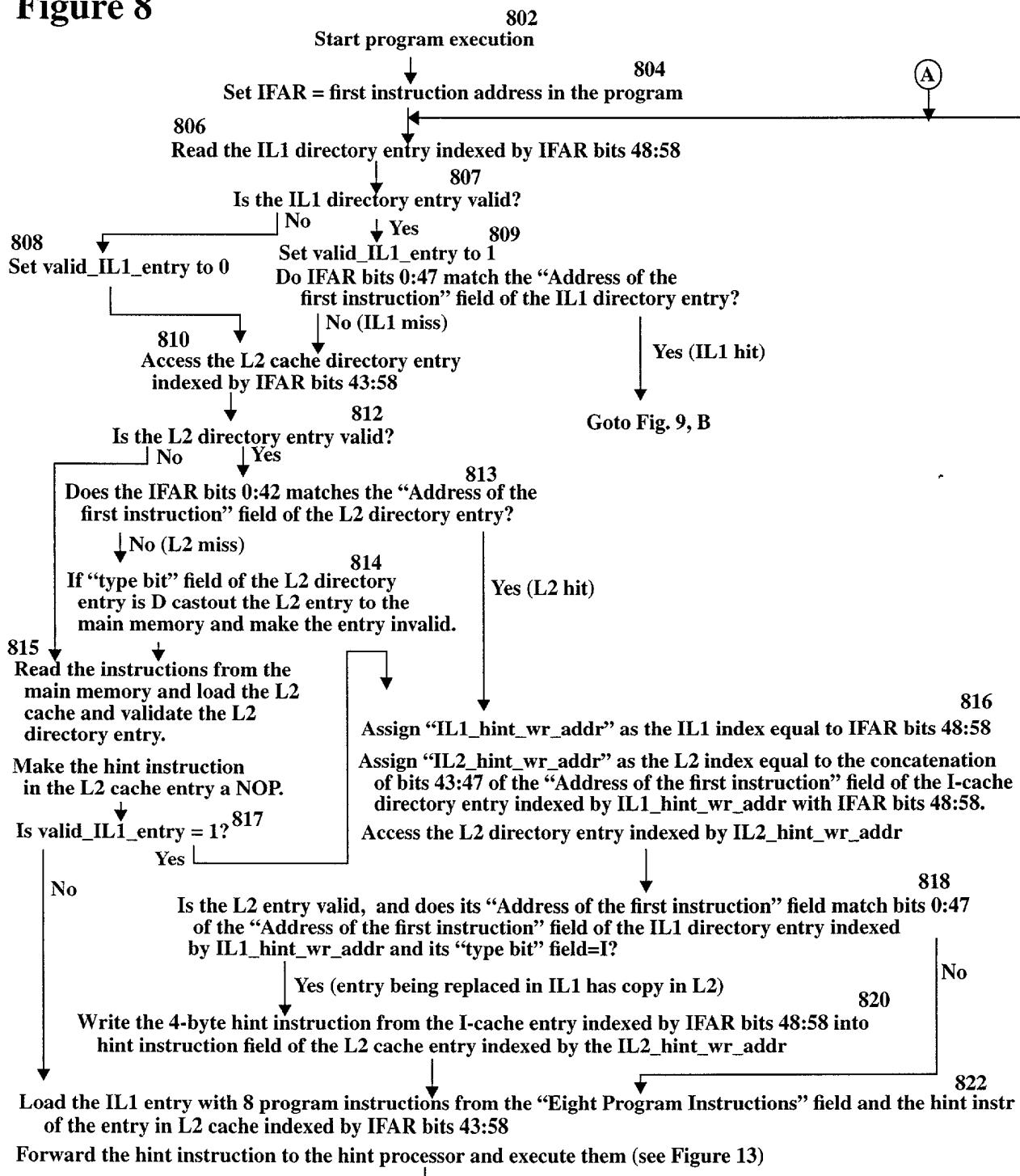


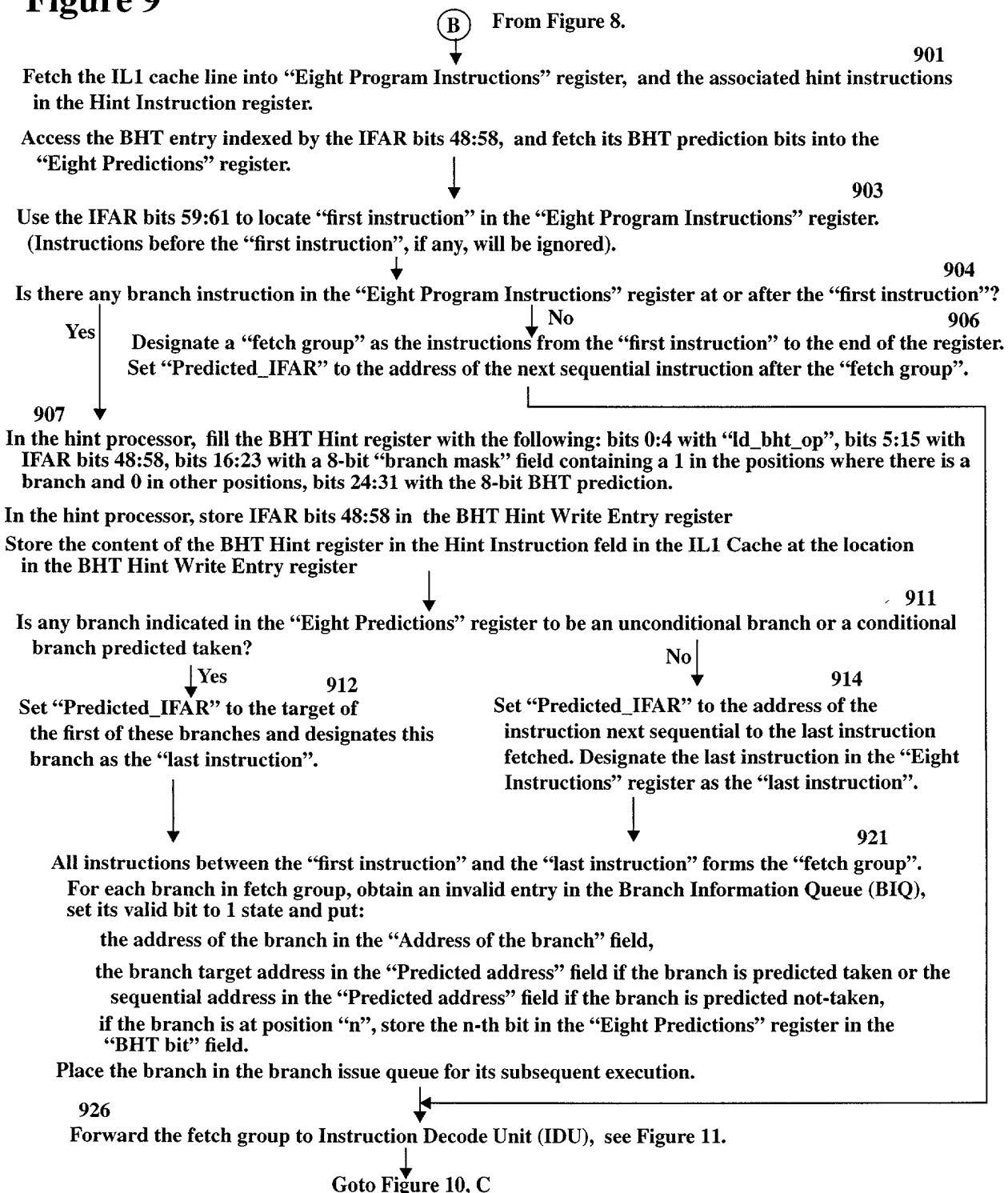
Figure 9

Figure 10
Next IFAR determination logic

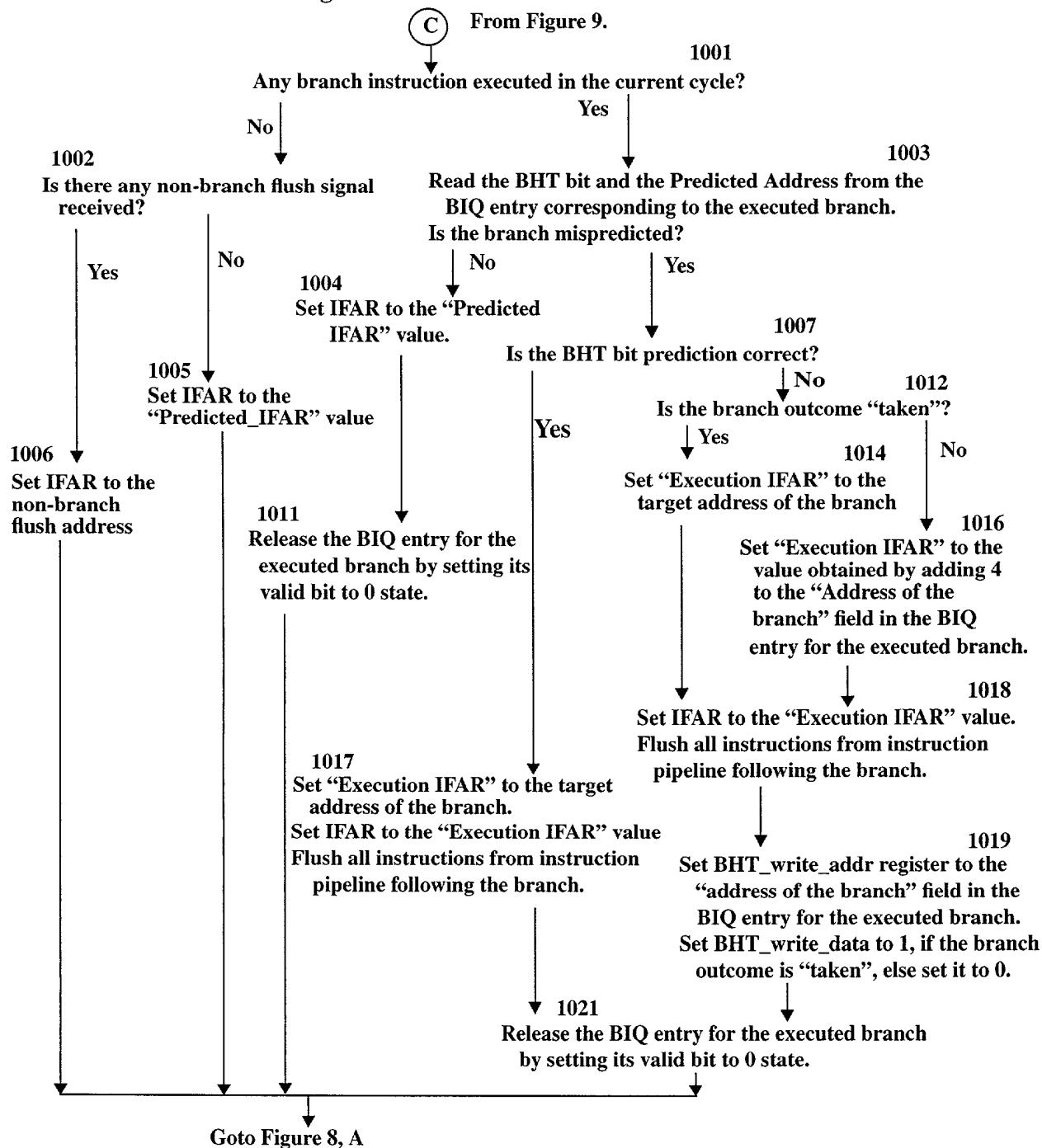


Figure 11
Instruction Decode and Dispatch

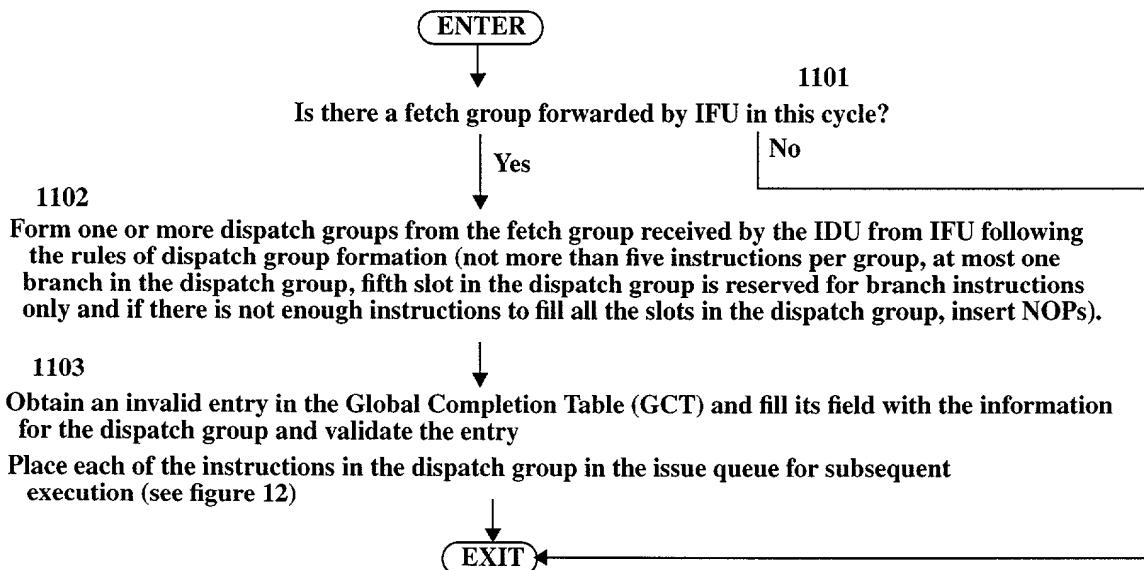


Figure 12

Instruction issue and instruction execution

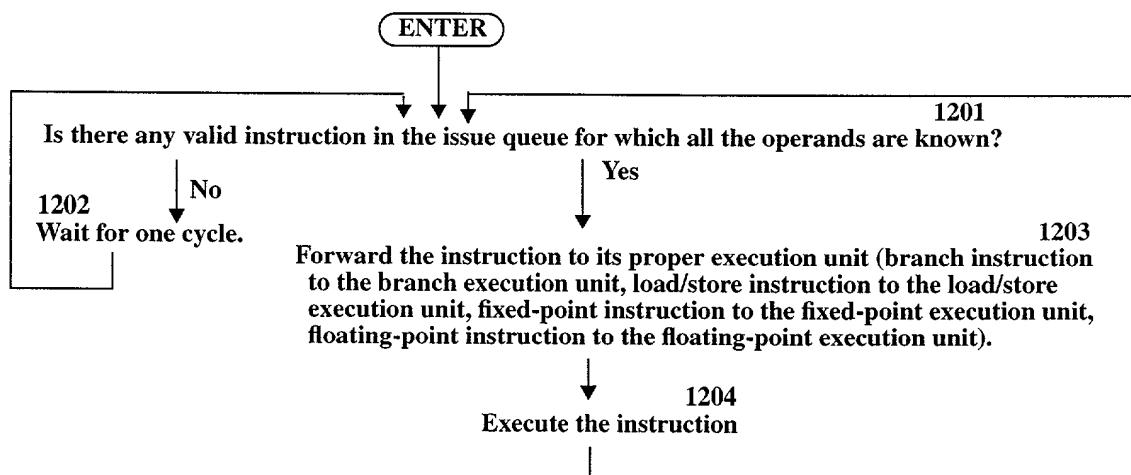


Figure 13
Execution in the Hint Processor for each IFAR cycle

